1. (once amended) A method of receiving a wireless transmission comprising the steps of:

inverting the polarity of an incoming waveform on every one half clock cycle of a conversion clock to produce a commutated waveform, translating said incoming waveform downward in frequency; and,

converting said commutated waveform to a series of representative digital values using a delta-sigma modulator clocked by said conversion clock.

7. (once amended) A receiver comprising:

a continuous time commutator configured to be coupled to a digital conversion clock and configured to invert [a]the polarity of an incoming signal applied to an input port on every half clock cycle of said digital conversion clock and translating said incoming signal downward in frequency to produce a commutated signal at an output port; and

a delta-sigma modulator having a clock input port coupled to said digital conversion clock, having a signal input port coupled to said output port of said continuous time commutator and having an output port configured to produce a series of digital values representative of a modulation waveform carried by said incoming signal.

13. (once amended) A circuit comprising:

a linearizing operational amplifier in a non-inverting unity follower configuration, configured to receive an incoming waveform;

a transistor network having a first input coupled to an output of said linearizing operational amplifier and having a second input coupled to said incoming waveform, said linearizing operational amplifier and said first complementary transistor network configured to

produce a pair of complementary currents that are linearly related to an input voltage of said incoming waveform;

a first current source coupled to said transistor network and configured to provide a fixed current through said first transistor network;

a commutator network coupled to a clock signal and coupled to said pair of complementary currents that are linearly related to said input voltage level of said incoming waveform such that said incoming waveform is translated in frequency;

a second current source configured to produce a fixed current; and

a switching network coupled to said second current source, having complementary input ports configured to be coupled to logic values and configured to produce complementary switched currents, wherein said complementary switched currents are coupled to said commutator network in order to control together complementary voltage outputs produced by the circuit.

14. (once amended) An apparatus [o]for receiving a wireless transmission comprising:

means for inverting the polarity of an incoming waveform on every one half clock cycle of a conversion clock and translating said incoming waveform downward in frequency to produce a commutated waveform; and

means for converting said commutated waveform to a series of representative digital values using a delta-sigma modulator clocked by said conversion clock.

Independent claims 1, 7, 13 and 14 have been rewritten to include translating the incoming waveform downward in frequency. It is believed that inclusion of this phrase in each of the independent claims avoids the prior art cited by the Examiner and places each and their corresponding dependent claims in a condition for allowance.

Support for amending each independent claim to include the phrase "translating said incoming waveform downward in frequency" can be found in the specification at page 9 line 24 to page 10, line 25.

The Examiner may be correct that the negative unity gain amplifier 41 and the switches 43 and 45 together can be considered as an inverter commutator (Office Action page 5 referring to Kotowski). However, if this assumption is made, it must take into account the intended purpose of the Kotowski reference, that being to provide offset and phase correction in delta-sigma modulators (Col 3, lines 8-9) utilizing a switching technique during different sampling periods to eliminate the effect of DC offsets (Col 3, lines 12-14).

Kotowski teaches (Col 6, lines 18-58) that when switches 43 and 49 are closed during one half period of the inverter clock, the output bit stream of the offset and phase correction delta-sigma modulator 20 represents an analog input signal: 01 = A * V1 + Voff and during the opposite half period of the inversion clock when switches 45 and 51 are closed, the output bit stream of the offset and phase correction delta sigma modulator represent a second analog input signal 02 = A * V1 - Voff. Kotowski concludes that by summing N values of 01 and N values of 02 that contribution of DC offset (Voff) is eliminated (Col 6, lines 52-60).

The Kotowski reference further teaches that for the offset and phase correction delta-sigma modulator to operate, the input signal 22 must be a baseband signal that includes zero frequency and that the inverter clock rate must be much less than the conversion clock rate in order to facilitate measurement of 01 and 02 to within an acceptable error (Col 5, lines 35-40).

The switches 43, 45, 49 and 51 (Kotowski Fig.3) clearly can not be operated at the same clock rate as the delta-sigma modulator because the inverter clock rate is less than the conversion clock rate in order to facilitate measurement of 01 and 02 to within an acceptable error. Thus, the Kotowski reference does not teach usage of the switches 43, 45, 49, 51 and inverting amplifier 41 to produce a "commutating waveform" as recited in claim 1.

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